



UNITED STATES PATENT AND TRADEMARK OFFICE

fl
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/408,149	09/29/1999	BHIMSEN BHANJOIS	07575/034001	3652
26181	7590	12/29/2005	EXAMINER	
FISH & RICHARDSON P.C. PO BOX 1022 MINNEAPOLIS, MN 55440-1022			ALI, SYED J	
			ART UNIT	PAPER NUMBER
			2195	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/408,149	BHANJOIS ET AL.
	Examiner	Art Unit
	Syed J. Ali	2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 15 August 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1,4-11,14-21,24-31 and 33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1,4-7,9-11,14-17,19-27,29-31 and 33 is/are rejected.

7) Claim(s) 8,18 and 28 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed August 15, 2005. Claims 1, 4-11, 14-21, 24-31, and 33 are presented for examination.
2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior office action.

Claim Objections

3. **Claims 1 is objected to because of the following informalities:**
 - a. In claim 1, “on machine readable medium” should read “on a machine readable medium”.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. **Claims 1, 4, 11, 14, 21, 24, 28, and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**
5. In claims 1, 4, 11, 14, 21, 24, and 31, there is ambiguity regarding the term “the operating system.” For instance, claim 1 is directed to “an operating system” and later recites that the one or more kernels execute “an operating system.” Thus, the limitation pertaining to “the operating system” being a time-sliced operating system or “operating system” being Unix is ambiguous

and subject to multiple interpretations. That is, it isn't clear whether "the operating system" is the operating system comprising a microkernel or the operating system being executed by a kernel as a dependent process of the operating system comprising a microkernel.

6. In claims 1, 11, 21, and 31, there is ambiguity regarding the term "the process." For instance, claim 1 indicates that "each process" executed by the non-preemptive microkernel only relinquishes the processor for "a higher priority process" when "the process" blocks or requests preemption. "The process" could be construed as either the executing process or the higher priority process. It seems as though the "executing process" is intended. The claims should be amended to resolve the ambiguity.

7. **The following terms lack antecedent basis:**

a. In line 2 of claim 28, "PID." Claim 27 defines a "PID" as a process identifier, but claim 28 depends from claim 21, which makes no mention of a "PID" or "process identifier."

Claim Rejections - 35 USC § 103

8. **Claims 1, 4, 6-7, 9-11, 14, 16-17, 19-21, 24, and 26-27, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur et al. (USPN 5,742,825) (hereinafter Mathur).**

9. As per claim 1, Mathur teaches the invention as claimed, including an operating system, tangibly stored on a machine readable medium, the operating system comprising:

a non-preemptive microkernel executing two or more processes in accordance with a non-preemptive scheduling scheme (col. 2 line 62 - col. 3 line 8; col. 6 lines 52-55; Fig. 1 element 20, wherein a microkernel is a simple abstraction over hardware, and Mathur describes the operating system as a modification of the Windows non-preemptive scheduling scheme), wherein each process executed by the non-preemptive microkernel relinquishes a processor for a higher priority process to execute only when the process blocks or explicitly requests to be preempted (col. 12 line 65 - col. 13 line 12, wherein all processes run under the Windows non-preemptive kernel, which only switches between processes when the process makes a yield call); and

one or more kernels each being executed as a process by the non-preemptive microkernel (col. 7 lines 40-56; Fig. 1 element 26; Fig. 2 elements 40, 42, the Windows kernel and the Office Machine OS kernel are part of the overall non-preemptive microkernel),

wherein at least one of the one or more kernels executes an operating system as a dependent process (col. 7 line 40 - col. 8 line 8, wherein the Windows kernel runs the Windows API), the operating system being a time-sliced operating system or a time-sliced microkernel (col. 15 line 59 - col. 16 line 9, the main operating system, Windows, is time-sliced and schedules foreground and background processes in alternating time-slices).

10. Examiner notes that previous rejections had been made over Mathur and were withdrawn. However, after reconsidering the references, Examiner believes the previous rejections were withdrawn in error. First, it is noted that the claim language suggests some slightly different

features from Mathur, but a brief explanation will show how Mathur does indeed read upon the claims, or at the least, the claims are an obvious modification of Mathur. There are two distinctions that require addressing: (1) is the claimed “non-preemptive microkernel” necessarily distinct from the overall “operating system”; and (2) can a process be forced to block or request preemption, or must it voluntarily yield without any input from the scheduler?

The first question can be disposed of rather easily. There is nothing precluding the claimed “operating system” from being the same as the “non-preemptive microkernel”. It is well known in the art that a microkernel is a layer of abstraction that rests over the system hardware. Mathur clearly shows the operating system in such an arrangement in Fig. 1. Since the operating system is a microkernel, it remains to be determined if it is non-preemptive. Mathur indicates that the operating system essentially modifies the non-preemptive scheduling scheme of Windows by adding preemptive scheduling for real-time processes. It can be said with certainty that the foreground processes are non-preemptive; this is made clear by Fig. 2 element 70. However, there is preemptive functionality, which directly leads to the second question presented above.

The claim recites that the executing process only relinquishes the processor when it blocks or requests to be preempted. On the other hand, Mathur clearly indicates that real-time processes that have hard deadlines must preempt the running process, such that it can be executed immediately. However, Examiner believes that the manner of implementing this preemption reads on the claim language. Read broadly, “the process blocks or explicitly requests to be preempted” indicates that preemption is permitted, but the executing process must request it. There is nothing in the claim that requires the request for preemption be performed

independently of any scheduler input. Mathur notes that the Windows API treats all processes in a non-preemptive manner, i.e. it will not consider scheduling another process until the executing process makes a yield call. The preemptive scheduler thus provides real-time capability by issuing a directed yield and block function to tell the executing process to yield. Thus, the executing process relinquishes the process by blocking, though it is told to block by the scheduler. Again, nothing in the claim language disallows the executing process from being told to block.

11. As per claim 4, Mathur does not specifically teach the invention as claimed, including the operating system of claim 2, wherein the operating system is Unix. However, Mathur does teach scheduling mechanisms and interprocess communication that is performed in a very similar manner to those of the Unix operating system. Mathur even explicitly states that the Windows kernel implements features that are well known to the Unix operating system (col. 9 lines 26-43). Therefore, “Official Notice” is taken that it would have been obvious to one of ordinary skill in the art that the scheduling techniques of Mathur could be equally applied to a Unix operating system as opposed to the Windows operating system since it would allow the technique to be used on a wider variety of systems. Referring to Fig. 2 of Mathur, the Windows kernel (element 42) along with the other Windows modules (elements 44 and 64) would need to be swapped out for the corresponding Unix modules, and would allow the benefits achieved by Mathur to apply to a greater number of computational platforms.

12. As per claim 6, Mathur teaches the invention as claimed, including the operating system of claim 1, wherein each of the two or more processes executed by the non-preemptive microkernel communicate using one or more messages (col. 9 lines 3-25).

13. As per claim 7, Mathur teaches the invention as claimed, including the operating system of claim 1, wherein each of the two or more processes executed by the non-preemptive microkernel has a unique process identifier [PID] (col. 19 line 64 - col. 20 line 7).

14. As per claim 9, Mathur teaches the invention as claimed, including the operating system of claim 1, wherein each of the two or more processes executed by the non-preemptive microkernel never terminates (col. 13 lines 13-32).

15. As per claim 10, Mathur teaches the invention as claimed, including the operating system of claim 1, wherein one of the one or more kernels is a microkernel (col. 7 lines 40-56).

16. As per claims 11, 14, and 16-20, Mathur teaches the invention as claimed, including a method for implementing the operating system of claims 1, 4, and 6-10, respectively (col. 3 lines 23-29).

17. As per claims 21, 24, and 26-30, Mathur teaches the invention as claimed, including a computer system for implementing the operating system of claims 1, 4, and 6-10, respectively (col. 5 lines 5-12).

18. **Claims 5, 15, 25, 31, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur in view of Hitz et al. (USPN 5,845,579) (hereinafter Hitz).**

19. As per claim 5, Hitz teaches the invention as claimed, including the following limitations not shown by Mathur:

the operating system of claim 1, wherein each of the two or more processes executed by the non-preemptive microkernel has its own stack (col. 11 line 64 - col. 12 line 21).

20. It would have been obvious to one of ordinary skill in the art to combine Mathur with Hitz since the operating system of Mathur swaps out the contents of the processor stack each time that an interrupt operation is performed. This is due to the fact that each process does not have an individual stack. Thus, each time a context switch occurs, the contents need to be swapped out, incurring a great deal of overhead. It would be advantageous to preserve the contents of the stack, such that when a process is resumed, no context switch is necessary. Hitz provides a framework for each process to have its own execution stack, thereby reducing the overhead costs of an interrupt operation.

21. As per claim 15, Mathur teaches the invention as claimed, including a method for implementing the operating system of claim 5 (col. 3 lines 23-29).

22. As per claim 25, Mathur teaches the invention as claimed, including a computer system for implementing the operating system of claim 5 (col. 5 lines 5-12).

23. As per claim 31, Mathur teaches the invention as claimed, including a computer, comprising:

a non-preemptive microkernel executing two or more processes in accordance with a non-preemptive scheduling scheme (col. 1 line 59 - col. 2 line 17; col. 2 line 62 - col. 3 line 4; col. 3 lines 30-47), wherein each process executed by the non-preemptive microkernel is only interrupted for a higher priority process to execute when the process blocks or explicitly requests to be preempted (col. 2 line 62 - col. 3 line 4; col. 12 line 65 - col. 13 line 49); and

one or more kernels each being executed as a process by the non-preemptive microkernel (col. 7 lines 10-30; col. 7 lines 40-56),

wherein at least one of the one or more kernels executes an operating system as a dependent process (col. 7 lines 40-56), the operating system being a time-sliced operating system or a time-sliced microkernel (col. 15 line 59 - col. 16 line 9).

24. Hitz teaches the invention as claimed, including the following limitations not shown by Mathur:

an interconnect bus (Abstract);

one or more processors coupled to the interconnect bus and adapted to be configured for server-specific functionalities including network processing, file processing, storage processing and application processing (Abstract);

a configuration processor coupled to the interconnect bus and to the processors, the configuration processor dynamically assigning processor functionalities upon request (col. 19 lines 7-26); and

one or more storage devices coupled to the processors and managed by a file system (Fig. 1, elements 161, 162, 241, and 242).

25. As per claim 33, Mathur teaches the invention as claimed, including the computer of claim 31, wherein the non-preemptive microkernel executes a network switch operating system as a dependent process (col. 8 lines 33-50).

Allowable Subject Matter

26. **Claims 8, 18, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.**

Response to Arguments

27. **Applicant's arguments with respect to claims 1, 4-11, 14-21, 24-31, and 33 have been considered but are moot in view of the new grounds of rejection.**

Conclusion

28. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J. Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T. An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Syed Ali
December 13, 2005


MENG-AI T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2200